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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,563	09/15/2003	Michael Ryan Davis	200309569-1	9738

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HEWLETT PACKARD COMPANY  
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INTELLECTUAL PROPERTY ADMINISTRATION  
FORT COLLINS, CO 80527-2400

EXAMINER
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SURYAWANSHI, SURESH

ART UNIT	PAPER NUMBER
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2115

MAIL DATE	DELIVERY MODE
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07/18/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/662,563	<b>Applicant(s)</b> DAVIS ET AL.	
	<b>Examiner</b> Suresh K. Suryawanshi	<b>Art Unit</b> 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 5/2/07 amendment.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 10-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13 is/are allowed.
- 6) ☒ Claim(s) 1-4, 10, 11 and 14 is/are rejected.
- 7) ☒ Claim(s) 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. Claims 1-5 and 10-14 are presented for examination.

#### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 10-11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Fish et al (US 2001/0042243; hereinafter Fish).

4. As per claim 1, Fish discloses a computer system having a plurality of processors within a cell, the cell comprising:

a processor type register [Fig. 3; processor type; paragraph 0024; the processor identifier (processor type) may be either hardware or software implemented],

at least one primary processor [Fig. 2; PU12],

a management subprocessor [Fig. 2 and 3; paragraphs 0019, 0022; here a management subprocessor is implemented through software for determining which processor type PU 12 is],

an EEPROM [paragraph 0020; FLASH memory],

and mapping hardware coupling the plurality of processors to the EEPROM [Fig. 2 and 3; paragraphs 0017-0022, 0030-0031];

wherein at system boot the management subprocessor reads the processor type register to determine an appropriate boot image of a plurality of boot images recorded within the EEPROM, and configures the mapping hardware to map the appropriate boot image into boot address space of the at least one primary processors of the cell [Fig. 2 and 3; paragraphs 0017-0022, 0024, 0030-0031 and 0033; clearly Fig. 3 illustrates how a management subprocessor (here a software program acting as a management subprocessor) determines a processor type and then configures the mapping hardware (gates 108 or 109) to map the appropriate boot image to the processor].

5. As per claim 2, Fish discloses a method of providing firmware to a processor of a cell of a cellular computer system comprising the steps:

reading a processor type register [Fig. 3; processor type; paragraph 0024; the processor identifier (processor type) may be either hardware or software implemented];

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determining a processor instruction set architecture from information read from the processor type register [Fig. 2 and 3; paragraphs 0019, 0022; determining which processor type PU 12 is];

selecting a compatible boot image from a plurality of boot images, the plurality of boot images contained within an EEPROM of the cell, where each boot image has associated boot-image information [Fig. 2 and 3; clearly shows having plurality of boot images for a plurality of processor types]; and

configuring mapping hardware to map the appropriate boot image of the EEPROM into boot address space of the processor [Fig. 2 and 3; paragraphs 0017-0022, 0024, 0030-0031 and 0033; clearly Fig. 3 illustrates how a management subprocessor (here a software program acting as a management subprocessor) determines a processor type and then configures the mapping hardware (gates 108 or 109) to map the appropriate boot image to the processor].

6. As per claim 3, Fish discloses the steps of reading a processor type register and selecting a compatible boot image are performed by a management coprocessor of the cell [Fig. 2 and 3; paragraphs 0017-0022, 0024, 0030-0031 and 0033; clearly Fig. 3 illustrates how a management subprocessor (here a software program acting as a management subprocessor) determines a processor type and then configures the mapping hardware (gates 108 or 109) to map the appropriate boot image to the processor].

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7. As per claim 10, Fish discloses that the boot images include boot images for more than one family of processor instruction set architectures [Fig. 2 and 3; paragraphs 0019, 0022; different processor types].

8. As per claim 11, Fish discloses that the computer system is a heterogeneous cellular computer system [Fig. 2 and 3; paragraphs 0019, 0022; having different processor types].

9. As per claim 14, Fish disclose

reading information from a processor type register into a management subprocessor [Fig. 3; processor type; paragraph 0024; the processor identifier (processor type) may be either hardware or software implemented];

determining a processor instruction set architecture from the information read from the processor type register [Fig. 2 and 3; paragraphs 0017-0022, 0024, 0030-0031 and 0033; clearly Fig. 3 illustrates how a management subprocessor (here a software program acting as a management subprocessor) determines a processor type];

selecting a compatible boot image from a plurality of boot images, the plurality of boot images contained within an EEPROM of the cell, where each boot image has associated boot image information, the step of selecting a compatible boot image being performed by the

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management subprocessor [Fig. 2 and 3; paragraphs 0017-0022, 0024, 0030-0031 and 0033; clearly Fig. 3 illustrates how a management subprocessor (here a software program acting as a management subprocessor) determines a processor type and then configures the mapping hardware (gates 108 or 109) to map the appropriate boot image to the processor]; and

configuring mapping hardware to map the compatible boot image of the EEPROM into boot address space of the first processor [Fig. 2 and 3; paragraphs 0017-0022, 0024, 0030-0031 and 0033; clearly Fig. 3 illustrates how a management subprocessor (here a software program acting as a management subprocessor) determines a processor type and then configures the mapping hardware (gates 108 or 109) to map the appropriate boot image to the processor];

wherein the boot images include boot images for more than one family of processor instruction set architectures [Fig. 2 and 3; paragraphs 0019, 0022; having different processor types and firmware images].

### ***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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11. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fish et al (US 2001/0042243; hereinafter Fish) in view of Thangadurai (US Patent 6,748,526<sup>1</sup>).

12. As per claims 4-5, Fish discloses the invention substantially. Fish does not expressly disclose about checking version information of the firmware image and making sure it is compatible to the processor type. However, Thangadurai clearly discloses verifying the version information of the firmware image and making sure it is compatible with the processor [col. 1, lines 36-43; col. 2, lines 46-51; col. 3, lines 7-12, 54-67; col. 5, lines 1-17, 49-64; col. 6, lines 6-8, 16-20]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to match an appropriate firmware image to a processor type. Moreover, Thangadurai discloses how to verify version and make sure it is compatible will clearly enhance the disclosure of Fish. Fish disclosure will clearly be benefited with the knowledge how to verify version number and check compatibility.

***Allowable Subject Matter***

13. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claim 13 allowed.

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<sup>1</sup> Prior art cited by the examiner in the prior office action.



***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Suresh K Suryawanshi